IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: William A. Harris

Title: PRECISION PHASE GENERATOR

Docket No.: H26054US
Filed: December 29, 2000
Examiner: Cassandra F. Cox

Serial No.: 09/751,610
Due Date: January 7, 2006
Group Art Unit: 2816

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
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(GENERAL)

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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PATENT

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APPEAL BRIEF UNDER 37 CFR § 41.37

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on July 26, 2005, from the Final Rejection of claims 1-3, 20-24, 26-29, 31-37, 39-45, 47 and 48 of the above-identified application, as set forth in the Final Office Action mailed on April 28, 2005.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of 500.00 which represents the requisite fee set forth in 37 C.F.R. § 41.2(b)(2). The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims.

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, HONEYWELL INTERNATIONAL INC.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings known to the appellant which will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

Claims 1-3, 20-24, 26-29, 31-37, 39-45 and 47-48 are pending in the application, and are rejected. Claims 1-3, 20-24, 26-29, 31-37, 39-45 and 47-48 are being appealed.

4. STATUS OF AMENDMENTS

No Amendment has been filed by the appellant subsequent to the final Office Action dated April 28, 2005.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The following is a concise explanation of the subject matter defined in each of the independent claims involved in the appeal. Claim elements are identified at least once by reference character and by the page and line in the specification where the element may be found.

Claim 1 recites a circuit for dividing an input clock signal into N clock signals having a relative phase separation of 360°/2N, where N is a positive integer, the circuit including a phase lock loop circuit (102, page 4, line 14) receiving an input signal (104, page 4, line 14) having a frequency F_0 and providing an output signal (108, page 4, lines 19-20) having a frequency $2NF_0$, a Johnson counter (104, page 4, line 22) having N JK flip-flops (220, 222, 224, 226, page 5, line 19) connected to receive as an input the output signal of the phase lock loop circuit and providing an output signal as an error signal to the phase lock loop circuit, said Johnson counter including an input JK flip-flop (220, page 5, line 19), an output JK flip-flop (226, page 5, line 19), and a plurality of middle JK flip-flops (222, 224, page 5, line 19), each JK flip-flop having a J input, a K input, a clock input coupled to receive the output signal having the frequency $2NF_0$ from the phase lock loop circuit, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, and the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop, and said Johnson counter also being connected for providing at least two output signals from at least two of the N JK flip-flops of the Johnson counter as clock signals each having a phase displaced from the phase of the other 360/2N°.

Claim 20 recites a method for generating at least two clock signals displaced from each other by a predetermined phase shift of 360°/2N, where N is a positive integer, the method including applying a clock signal (104, page 4, line 14) to a signal input of a phase lock loop circuit (102, page 4, line 14) at a desired clock frequency, applying a

feedback signal to a second input (106, page 4, line 16) of the phase lock loop circuit, generating an output signal (108, page 4, lines 19-20) of the phase lock loop circuit having a frequency of $2NF_0$, coupling the output signal of the phase lock loop circuit to a clock input of each JK flip-flop of a Johnson counter (104, page 4, line 22) to provide the feedback signal to the second input of the phase lock loop circuit having a frequency corresponding to the frequency of the output signal of the phase lock loop circuit divided by 2N, the Johnson counter including N JK flip-flops (220, 222, 224, 226, page 5, line 19) including an input JK flip-flop (220, page 5, line 19), an output JK flip-flop (226, page 5, line 19), and a plurality of middle JK flip-flops (222, 224, page 5, line 19), each JK flip-flop having a J input, a K input, the clock input, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop, and coupling outputs of the JK flip-flops of the Johnson counter for use as phase shifted clock outputs.

Claim 32 recites a circuit to divide an input signal into multiple output clock signals, the circuit including a phase lock loop circuit (102, page 4, line 14) coupled to receive an input signal (104, page 4, line 14) having a frequency F_0 and coupled to provide an output signal (108, page 4, lines 19-20) having a frequency $2NF_0$, wherein N is a positive integer and a Johnson counter (104, page 4, line 22) having N JK flip-flops (220, 222, 224, 226, page 5, line 19) coupled to receive as an input the output signal of the phase lock loop circuit and coupled to provide an output signal as an error signal to the phase lock loop circuit, the Johnson counter also being coupled to provide at least two output signals from at least two of the N JK flip-flops of the Johnson counter as output clock signals, each output clock signal having a phase displaced from a phase of each other output clock signal by at least $360/2N°$, the Johnson counter including an input JK flip-flop (220, page 5, line 19), an output JK flip-flop (226, page 5, line 19), and a plurality of middle JK flip-flops (222, 224, page 5, line 19), each JK flip-flop having a J input, a K input, a clock input coupled to receive the output signal having the frequency

$2NF_0$ from the phase lock loop circuit, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, and the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop.

Claim 40 recites a method of generating multiple output clock signals including applying an input clock signal (104, page 4, line 14) having a frequency F_0 to a signal input of a phase lock loop circuit (102, page 4, line 14), applying a feedback signal to an error input (106, page 4, line 16) of the phase lock loop circuit, generating an output signal (108, page 4, lines 19-20) having a frequency $2NF_0$ from the phase lock loop circuit wherein N is a positive integer, coupling the output signal having the frequency $2NF_0$ from the phase lock loop circuit to a clock input of each JK flip-flop of a Johnson counter (104, page 4, line 22), the Johnson counter including N JK flip-flops (220, 222, 224, 226, page 5, line 19) including an input JK flip-flop (220, page 5, line 19), an output JK flip-flop (226, page 5, line 19), and a plurality of middle JK flip-flops (222, 224, page 5, line 19), each JK flip-flop having a J input, a K input, the clock input, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop, generating the feedback signal in the Johnson counter in response to the output signal having the frequency $2NF_0$ from the phase lock loop circuit, and generating an output clock signal from at least two of the N JK flip-flops of the Johnson counter, each output clock signal having a phase displaced from a phase of each other output clock signal by at least $360/2N°$.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Claims 1-3, 20-24, 26-29, 31-37, 39-45 and 47-48 stand rejected under 35 USC §103(a) as being unpatentable over Li (U.S. Patent No. 5,058,132) in view of Epstein (U.S. Patent No. 4,093,870) and Mano (Computer Engineering Hardware Design, 1988, pgs.130-132).

7. ARGUMENT

The Applicable Law

All of the pending claims were rejected under 35 U.S.C. §103:

> "A patent may not be obtained...if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art."[1]

The MPEP states the following with regard to rejections under 35 USC § 103:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. "[2]

The appellant respectfully submits that the final Office Action fails to make a *prima facie* showing of obviousness by failing to show motivation to combine Li, Epstein, and Mano and also fails to provide evidence of a reasonable expectation of success of the combination.

A Federal Circuit opinion states that the suggestion or motivation to combine references and the reasonable expectation of success must both be found in the prior art.[3]

Multiple Federal Circuit decisions emphasize the need for the PTO to furnish evidence in support of claim rejections. For example, the Federal Circuit addressed citation of "basic knowledge or common sense" in rejections in *In re Zurko*:

> "With respect to core factual findings in a determination of patentability, however, the Board [Board of Patent Appeals and Interferences] cannot simply reach conclusions based on its own understanding or experience – or on its assessment of what would be basic knowledge or common sense. Rather, the Board must point to some concrete evidence in the record in support of these findings."[4]

The Federal Circuit has particularly emphasized the need for the PTO to furnish evidence in support of claim rejections under 35 USC § 103 in *In re Lee*:

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[1] 35 U.S.C. § 103(a).
[2] MPEP 2143.
[3] MPEP 2143 citing *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).
[4] *In re Zurko*, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001).

> "When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness.....The factual inquiry whether to combine references must be thorough and searching....It must be based on objective evidence of record." [5]

The Federal Circuit stated that the "need for specificity pervades this authority" requiring a teaching, motivation, or suggestion to select and combine references.[6] The Federal Circuit has expressed this need for specificity in several cases:

> "[T]he best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.....the showing must be clear and particular." [7]

> "[E]ven when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination."[8]

> "[P]articular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed."[9]

A finding of a suggestion or motivation is part of the inquiry into the scope and content of the prior art under *Graham*:

> "Determining whether there is a suggestion or motivation to modify a prior art reference is one aspect of determining the scope and content of the prior art, a fact question subsidiary to the ultimate conclusion of obviousness."[10]

The Federal Circuit has emphasized the importance of a thorough investigation of the *Graham* factors for less complex technologies:

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[5] *In re Lee*, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).
[6] *In re Lee*, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).
[7] *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).
[8] *In re Rouffet,* 47 USPQ2d 1453, 1459 (Fed. Cir. 1998).
[9] *In re Kotzab,* 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).
[10] *Ruiz v. A.B. Chance Co.,* 57 USPQ2d 1161, 1167 (Fed. Cir. 2000). The factual inquiries made under 35 U.S.C. §103 are set out in *Graham v. John Deere Co.*, 148 USPQ 459 (1966), cited in *Ruiz*, 57 USPQ2d at 1165.

"The necessity of *Graham* findings is especially important where the invention is less technologically complex...In such a case, the danger increases that 'the very ease with which the invention can be understood may prompt one 'to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher.'"[11]

[11] *Ruiz v. A.B. Chance Co.*, 57 USPQ2d 1161, 1166 (Fed. Cir. 2000).

Rejection

Claims 1-3, 20-24, 26-29, 31-37, 39-45 and 47-48 stand rejected under 35 USC §103(a) as being unpatentable over Li (U.S. Patent No. 5,058,132) in view of Epstein (U.S. Patent No. 4,093,870) and Mano (Computer Engineering Hardware Design, 1988, pgs.130-132).

Each of the independent claims 1, 20, 32, and 40 recite, among other elements, a Johnson counter comprising an input JK flip-flop, an output JK flip-flop, and a plurality of middle JK flip-flops. The remaining claims are variously dependent on, and recite further features with respect to, the independent claims 1, 20, 32, and 40.

The applicant respectfully submits that the final Office Action has not identified prior art evidence of a suggestion for combining Li with Epstein and Mano, or evidence of a reasonable expectation of success of this combination.

Li relates to a clock distribution system and shows a circuit called a Johnson counter 114 in Figure 2. A prior Office Action stated that "Li does not disclose the particular design of the Johnson counter."[12] Epstein relates to an apparatus for testing reflexes and shows a circuit called a Johnson counter 54 in Figure 4. Epstein's Johnson counter 54 has only three JK flip-flops.

Mano describes different types of flip-flops, and contrasts the operation of each. Specifically, Mano describes JK flip-flops, D flip-flops, SR flip-flops, and T flip-flops.[13] Mano does not discuss Johnson counters, or the relative merits of different Johnson counters.

[12] Final Office Action dated April 7, 2004, page 2.
[13] Mano, page 131.

Neither Li nor Epstein show a Johnson counter comprising an input JK flip-flop, an output JK flip-flop, and a plurality of middle JK flip-flops as is recited in the independent claims 1, 20, 32, and 40. Mano does not show or discuss a Johnson counter. Therefore, even as combined, Li, Epstein, and Mano do not show the claimed invention.

There is also no clear and particular evidence of a suggestion or motivation to combine Li, Epstein, and Mano. The final Office Action stated that:

> "[I]t would have been obvious .... to implement the 5 stages (flip flop circuits) Johnson counter of Li with a five JK flip flop circuit arranged as in Epstein because JK flip flop is reliable thus preventing the counter from erroneous operation as taught by Mano." [14]

Epstein does not show a counter with five JK flip flops. Epstein's Johnson counter has only three JK flip-flops. More significantly, Mano does not show or discuss Johnson counters. Mano does not comment on the reliability of any particular Johnson counter, and does not teach that any particular Johnson counter suffers from erroneous operation. One skilled in the art would not be motivated by Mano to modify the Johnson counter of Li.

There is no evidence of the rationale stated in the final Office Action and quoted above for combining Li, Epstein, and Mano as is required by *In re Lee*. There is no showing of clear and particular evidence of a suggestion for combining Li, Epstein, and Mano as is required by *In re Dembiczak*.

The final Office Action has failed to show the multiple levels of suggestion needed to combine three references. The final Office Action has failed to show evidence of a suggestion to combine Li with Epstein, and then evidence of a suggestion to combine Mano with Li and Epstein.

The final Office Action has also not identified evidence of a reasonable expectation of success for this combination in the prior art as is required by MPEP 2143, *In re Vaeck* and *In re Lee*. There is no evidence of how the elements of Li, Epstein, and Mano are to be arranged and assembled together. The Federal Circuit has

[14] Final Office Action, page 3.

stated that all elements of a *prima facie* case of obviousness must be established in a rejection:

> "Omission of a relevant factor required by precedent is both legal error and arbitrary agency action." [15]

A *prima facie* case of obviousness can not be established against claims 1-3, 20-24, 26-29, 31-37, 39-45 and 47-48 without evidence of a reasonable expectation of success.

The final Office Action is improperly using hindsight in combining Li, Epstein, and Mano contrary to *In re Dembiczak.* This is a case where "the very ease with which the invention can be understood may prompt one 'to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher.'"[16] The court in *Ruiz* emphasized that "[t]he necessity of *Graham* findings is especially important where the invention is less technologically complex."[17]

The applicant respectfully submits that a *prima facie* case of obviousness against claims 1-3, 20-24, 26-29, 31-37, 39-45 and 47-48 has not been established in the final Office Action, and that claims 1-3, 20-24, 26-29, 31-37, 39-45 and 47-48 are in condition for allowance.

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[15] *In re Lee*, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).
[16] *Ruiz v. A.B. Chance Co.*, 57 USPQ2d 1161, 1166 (Fed. Cir. 2000).
[17] *Ruiz v. A.B. Chance Co.*, 57 USPQ2d 1161, 1166 (Fed. Cir. 2000).

8. SUMMARY

Request For Reversal

For the foregoing reasons, the appellant respectfully submits that the rejection of claims 1-3, 20-24, 26-29, 31-37, 39-45, 47 and 48 under 35 U.S.C. §103 was erroneous. Reversal of this rejection is respectfully requested, as well as the allowance of all the rejected claims.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

WILLIAM A. HARRIS

By his Representatives,

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Date 6 January 2006 By _____
Robert E. Mates
Reg. No. 35,271

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Dawn M. Pavle
Name

Dawn M. Pavle
Signature

CLAIMS APPENDIX

1. (Rejected) A circuit for dividing an input clock signal into N clock signals having a relative phase separation of 360°/2N, where N is a positive integer, the circuit comprising:

a phase lock loop circuit receiving an input signal having a frequency F_0 and providing an output signal having a frequency $2NF_0$;

a Johnson counter having N JK flip-flops connected to receive as an input the output signal of the phase lock loop circuit and providing an output signal as an error signal to the phase lock loop circuit, said Johnson counter comprising an input JK flip-flop, an output JK flip-flop, and a plurality of middle JK flip-flops, each JK flip-flop having a J input, a K input, a clock input coupled to receive the output signal having the frequency $2NF_0$ from the phase lock loop circuit, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, and the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop; and

said Johnson counter also being connected for providing at least two output signals from at least two of the N JK flip-flops of the Johnson counter as clock signals each having a phase displaced from the phase of the other 360/2N°.

2. (Rejected) The circuit of claim 1 wherein N =4.

3. (Rejected) The circuit of claim 1 wherein N=8.

4-19. (Canceled)

20. (Rejected) A method for generating at least two clock signals displaced from each other by a predetermined phase shift of 360°/2N, where N is a positive integer, the method comprising:

applying a clock signal to a signal input of a phase lock loop circuit at a desired clock frequency;

applying a feedback signal to a second input of the phase lock loop circuit;

generating an output signal of the phase lock loop circuit having a frequency of $2NF_0$;

coupling the output signal of the phase lock loop circuit to a clock input of each JK flip-flop of a Johnson counter to provide the feedback signal to the second input of the phase lock loop circuit having a frequency corresponding to the frequency of the output signal of the phase lock loop circuit divided by 2N, the Johnson counter comprising N JK flip-flops including an input JK flip-flop, an output JK flip-flop, and a plurality of middle JK flip-flops, each JK flip-flop having a J input, a K input, the clock input, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop; and

coupling outputs of the JK flip-flops of the Johnson counter for use as phase shifted clock outputs.

21. (Rejected) The method of claim 20 wherein N =4.

22. (Rejected) The circuit of claim 1 wherein the Johnson counter is coupled to provide a clock signal from each of the N JK flip-flops in response to the output signal having the frequency $2NF_0$, the error signal being one of the clock signals, the N clock signals having a relative phase separation of at least 360°/2N and each clock signal having a frequency F_0.

23. (Rejected) The circuit of claim 1 wherein the error signal and each clock signal has a frequency F_0.

24. (Rejected) The circuit of claim 1 wherein the phase lock loop circuit comprises:

a phase detector coupled to receive and compare the input signal having the frequency F_0 and the error signal from the Johnson counter and to provide an output signal corresponding to a phase difference between the input signal having the frequency F_0 and the error signal;

a low pass filter and a gain stage coupled to receive the output signal from the phase detector and to produce a control signal;

a voltage controlled oscillator coupled to the low pass filter and the gain stage to receive the control signal and coupled to the Johnson counter to produce the output signal having the frequency $2NF_0$ in response to the control signal.

25. (Canceled)

26. (Rejected) The circuit of claim 1 wherein each Q output and each complemented Q output of each JK flip-flop is coupled to provide a clock signal, the 2N clock signals having a relative phase separation of 360°/2N, and each clock signal having a frequency F_0.

27. (Rejected) The method of claim 20 wherein the feedback signal is one of the clock outputs, the clock outputs having a relative phase separation of at least 360°/2N and each clock output having a frequency F_0.

28. (Rejected) The method of claim 20, further comprising generating the feedback signal and each clock output with a frequency F_0.

29. (Rejected) The method of claim 20 wherein generating an output signal of the phase lock loop circuit comprises:

comparing the clock signal at the signal input and the feedback signal in a phase detector;

generating an output signal from the phase detector corresponding to a phase difference between the clock signal at the signal input and the feedback signal;

generating a control signal in a low pass filter and a gain stage in response to the output signal from the phase detector; and

generating the output signal of the phase lock loop circuit in response to the control signal in a voltage controlled oscillator coupled to the low pass filter and the gain stage.

30. (Canceled)

31. (Rejected) The method of claim 20, further comprising:

generating a clock output from each Q output and each complemented Q output of each JK flip-flop of the Johnson counter, the 2N clock outputs having a relative phase separation of 360°/2N, and each clock output having a frequency F_0.

32. (Rejected) A circuit to divide an input signal into multiple output clock signals, the circuit comprising:

a phase lock loop circuit coupled to receive an input signal having a frequency F_0 and coupled to provide an output signal having a frequency $2NF_0$, wherein N is a positive integer; and

a Johnson counter having N JK flip-flops coupled to receive as an input the output signal of the phase lock loop circuit and coupled to provide an output signal as an error signal to the phase lock loop circuit, the Johnson counter also being coupled to provide at least two output signals from at least two of the N JK flip-flops of the Johnson counter as output clock signals, each output clock signal having a phase displaced from a phase of each other output clock signal by at least 360/2N°, the Johnson counter comprising an

input JK flip-flop, an output JK flip-flop, and a plurality of middle JK flip-flops, each JK flip-flop having a J input, a K input, a clock input coupled to receive the output signal having the frequency $2NF_0$ from the phase lock loop circuit, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, and the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop.

33. (Rejected) The circuit of claim 32 wherein N is 4.

34. (Rejected) The circuit of claim 32 wherein N is 8.

35. (Rejected) The circuit of claim 32 wherein the Johnson counter is coupled to provide an output clock signal from each of the N JK flip-flops in response to the output signal having the frequency $2NF_0$, the error signal being one of the output clock signals, the N output clock signals having a relative phase separation of at least 360°/2N and each output clock signal having a frequency F_0.

36. (Rejected) The circuit of claim 32 wherein the error signal and each output clock signal has a frequency F_0.

37. (Rejected) The circuit of claim 32 wherein the phase lock loop circuit comprises:

a phase detector coupled to receive and compare the input signal having the frequency F_0 and the error signal from the Johnson counter and to provide an output signal corresponding to a phase difference between the input signal having the frequency F_0 and the error signal;

a low pass filter and a gain stage coupled to receive the output signal from the phase detector and to produce a control signal;

a voltage controlled oscillator coupled to the low pass filter and the gain stage to receive the control signal and coupled to the Johnson counter to produce the output signal having the frequency $2NF_0$ in response to the control signal.

38. (Canceled)

39. (Rejected) The circuit of claim 32 wherein each Q output and each complemented Q output of each JK flip-flop is coupled to provide an output clock signal, the 2N output clock signals having a relative phase separation of 360°/2N, and each output clock signal having a frequency F_0.

40. (Rejected) A method of generating multiple output clock signals comprising:

applying an input clock signal having a frequency F_0 to a signal input of a phase lock loop circuit;

applying a feedback signal to an error input of the phase lock loop circuit;

generating an output signal having a frequency $2NF_0$ from the phase lock loop circuit wherein N is a positive integer;

coupling the output signal having the frequency $2NF_0$ from the phase lock loop circuit to a clock input of each JK flip-flop of a Johnson counter, the Johnson counter comprising N JK flip-flops including an input JK flip-flop, an output JK flip-flop, and a plurality of middle JK flip-flops, each JK flip-flop having a J input, a K input, the clock input, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop;

generating the feedback signal in the Johnson counter in response to the output signal having the frequency $2NF_0$ from the phase lock loop circuit; and

generating an output clock signal from at least two of the N JK flip-flops of the Johnson counter, each output clock signal having a phase displaced from a phase of each other output clock signal by at least 360/2N°.

41. (Rejected) The method of claim 40 wherein N is 4.

42. (Rejected) The method of claim 40 wherein N is 8.

43. (Rejected) The method of claim 40, further comprising generating an output clock signal from each of the N JK flip-flops of the Johnson counter, the feedback signal being one of the output clock signals, the N output clock signals having a relative phase separation of at least 360°/2N and each output clock signal having a frequency F_0.

44. (Rejected) The method of claim 40, further comprising generating the feedback signal and each output clock signal with a frequency F_0.

45. (Rejected) The method of claim 40 wherein generating an output signal having a frequency $2NF_0$ comprises:

comparing the input clock signal having the frequency F_0 and the feedback signal and in a phase detector;

generating an output signal from the phase detector corresponding to a phase difference between the input clock signal having the frequency F_0 and the feedback signal;

generating a control signal in a low pass filter and a gain stage in response to the output signal from the phase detector; and

generating the output signal having the frequency $2NF_0$ in response to the control signal in a voltage controlled oscillator coupled to the low pass filter and the gain stage.

46. (Canceled)

47. (Rejected) The method of claim 40, further comprising:

generating an output clock signal from each Q output and each complemented Q output of each JK flip-flop of the Johnson counter, the 2N output clock signals having a relative phase separation of 360°/2N, and each output clock signal having a frequency F_0.

48. (Rejected) The method of claim 20 wherein N =8.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.